In the Claims:

Pursuant to 37 C.F.R. §1.121 and the revised amendment practice effective July 30, 2003, please cancel clams 5, 6, 12, 13 and 17, and amend claims 1, 7-11 and 14-16 as indicated herein. Pursuant to 37 C.F.R. §1.121(c), a complete listing of all the claims in the application is provided immediately below.

COMPLETE LISTING OF ALL CLAIMS IN THE APPLICATION

1. (Currently amended) A frequency-sensitive electrical circuit, comprising:

first and second inputs;

at least one transformer circuit having a first winding connected to the first input and a second winding connected to the second input;

a first load connected in parallel to the first winding;

a second load connected in parallel to the second winding;

first and second outputs connected to the first and second windings, respectively; ~~and~~

a capacitor connected between the first and second outputs;

third and fourth inputs;

third and fourth outputs;

a parallel-connected third winding and second capacitor, connected between the third and the third output;

a parallel-connected fourth winding and third capacitor, connected between the fourth input and the fourth output, the third winding and the fourth winding being inductively coupled; and

a fourth capacitor connected between the third and fourth outputs;

wherein the third and fourth outputs form the first and second inputs, respectively.

2. (Original) The circuit of claim 1, wherein a signal carrying both voice and data information is received at the first and second inputs.

3. (Original) The circuit of claim 1, wherein the circuit filters a lower-frequency portion of a signal received at the first and second inputs.

4. (Original) The circuit of claim 1, wherein the circuit reduces the distortion of a signal received at the first and second inputs and delivered at the first and second outputs.

5. (Canceled).

6. (Canceled).

7. (Currently amended) ~~The circuit of claim 6, further comprising:~~ A frequency-sensitive electrical circuit, comprising:

a first stage having first and second inputs and first and second outputs, the first stage comprising

a parallel-connected first inductor and first resistor, connected between the first input and first output of the first stage,

a parallel-connected second inductor and second resistor, connected between the second input and second output of the first stage, the first and second inductors being inductively coupled, and

a first capacitor connected between the first and second outputs of the first stage; and

a second stage having first and second inputs and first and second outputs, the second stage comprising

a parallel-connected third inductor and second capacitor, connected between the first input and first output of the second stage,

a parallel-connected fourth inductor and third capacitor, connected between the second input and second output of the second stage, the third and fourth inductors being inductively coupled, and

a fourth capacitor connected between the first and second outputs of the second stage,

wherein the first and second outputs of the second stage form the first and second inputs of the first stage, respectively.

8. (Currently amended) ~~The circuit of claim 6, further comprising:~~ A frequency-sensitive electrical circuit, comprising:

a first stage having first and second inputs and first and second outputs, the first stage comprising

a parallel-connected first inductor and first resistor, connected between the first input and first output of the first stage,

a parallel-connected second inductor and second resistor, connected between the second input and second output of the first stage, the first and second inductors being inductively coupled, and

a first capacitor connected between the first and second outputs of the first stage; and

a second stage having first and second inputs and first and second outputs, the second stage comprising

a third inductor connected between the first input and first output of the second stage,

a fourth inductor connected between the second input and second output of the second stage, the third and ~~second~~ fourth inductors being inductively coupled, and

a second capacitor connected between the first and second outputs of the second stage,

wherein the first and second outputs of the second stage form the first and second inputs of the first stage, respectively.

9. (Currently amended) The circuit of ~~claim 6~~ claim 7, wherein a signal carrying both voice and data information is received at the first and second inputs of the first stage.

10. (Currently amended) The circuit of ~~claim 6~~ claim 7, wherein the circuit filters a lower-frequency portion of a signal received at the first and second inputs of the first stage.

11. (Currently amended) The circuit of ~~claim 6~~ claim 7, wherein the circuit reduces the distortion of a signal received at the first and second inputs of the first stage and delivered at the first and second outputs of the first stage.

12. (Canceled).

13. (Canceled).

14. (Currently amended) The circuit of ~~claim 13~~ claim 8, wherein a signal carrying both voice and data information is received at the first and second inputs of the first stage.

15. (Currently amended) The circuit of ~~claim 13~~ claim 8, wherein the circuit filters a lower-frequency portion of a signal received at the first and second inputs of the first stage.

16. (Currently amended) The circuit of ~~claim 13~~ claim 8, wherein the circuit reduces the distortion of a signal received at the first and second inputs of the first stage and delivered at the first and second outputs of the first stage.

17. (Canceled).